**ECE 6213 – Design of VLSI Circuits**

**Fall 2022 – The George Washington University – Dr. Jerry Wu**

**Osama Yousuf – HW 1**

**Problem 1 – 40 points**

* **Ch-5 – Problem 13: Verify the functionality of *Universal\_Shift\_Reg* in Example 5.45.**

Verilog code: *universal\_shift\_reg.v*

Text

Description automatically generated

Testbench: *universal\_shift\_reg\_tb.v*

*Graphical user interface, text

Description automatically generated*

*Text

Description automatically generated*

Output waveform from my testbench:

A screenshot of a computer

Description automatically generated with medium confidence

Corresponding waveform from the book – the input and output waveforms align one-to-one.

A sheet of music

Description automatically generated with low confidence

* Ch5 - Problem 14: Write a Verilog description of the circuit shown in Figure P5-15 and verify that the circuit's output, P odd, is asserted if successive samples of V \_in have an odd number of Is.

A screenshot of a computer

Description automatically generated